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**1 .Introduction**

Digital to analogue converter (DAC) and analogue to digital converter (ADC), based on the R-

2R ladder network, are widely used. The technique provides high speed, high accuracy (over a

Wide temperature range) and relatively low cost. This is mainly because the FET switches and thin film resistors can be integrated, with accurately matched ratios and temperature coefficients, on to a single silicon chip with a low cost process. Some devices also include an optional voltage reference and an operational amplifier for a reduced system chip count.

In this exercise one DAC and one ADC, based on the R-2R ladder network, are to construct from basic components. The designs are intended to demonstrate the working principles and the side effects involved. The exercise does not focus on converter applications.

**Objectives**

. To understand the principles of operation of R-2R converters.

. Application of the theoretical knowledge in determining converter parameters.

# 2. Experiments

## 2.1 Unipolar Binary Coded 4 bit DAC



Figure 1 Unipolar dual coded 4-bit DAC with voltage output (Source: Task)

### Preparation

First, calculate the R9 resistor of the amplifier (see Figure 1) :

Vref‘ = 5V

Vout = 4V

In order to calculate the resistor R9 the equivalent circuit diagram of a simple inverting amplifier considered (Figure 2). Here, the gain is given by:

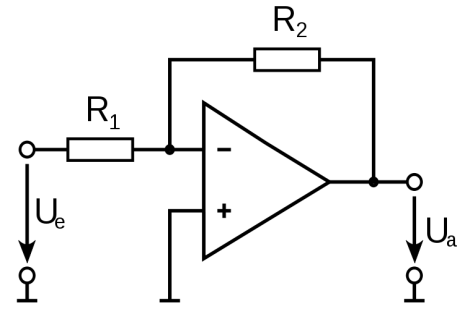


Figure 2 Equivalent circuit diagram as a simple inverting amplifier

To obtain R1 (Figure 2), the resistors must R1 to R8 (Figure 1) will collectively an input resistor net.

This yields the following equation for the gain of the circuit:

### 2.1.1 Static transfer characteristic

For each of the 16 values possible at the digital input (Z[0..15]; i.e. I[3"0] : LLLL"HHHH)

Measure the analogue output V6ul using a DMM. Choose a DMM measuring rate which gives

You 4 digit resolution after decimal point (otherwise you would not get a sufficiently accurate

Result when calculating nonlinearity).

You may employ double-throw switches as the source of digital input with L : 0 V and H : 5

V.

In the laboratory, the following values ​​were recorded:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit 1 | Bit 2 | Bit 3 | Bit 4 | Vout |
| 0 | 0 | 0 | 0 | 0.00006 V |
| 0 | 0 | 0 | 1 | -0.25275V |
| 0 | 0 | 1 | 0 | -0.5051V |
| 0 | 0 | 1 | 1 | -0.7579V |
| 0 | 1 | 0 | 0 | -1.0107V |
| 0 | 1 | 0 | 1 | -1.2635V |
| 0 | 1 | 1 | 0 | -1.5159V |
| 0 | 1 | 1 | 1 | -1.7688V |
| 1 | 0 | 0 | 0 | -2.0208V |
| 1 | 0 | 0 | 1 | -2.2736V |
| 1 | 0 | 1 | 0 | -2.5260V |
| 1 | 0 | 1 | 1 | -2.7801V |
| 1 | 1 | 0 | 0 | -3.0332V |
| 1 | 1 | 0 | 1 | -3.286V |
| 1 | 1 | 1 | 0 | -3.538V |
| 1 | 1 | 1 | 1 | -3.791V |

Table 1 measured the output voltage

### 2.1.2 Dynamic transmission behavior

All power switches are now shorted together and connected to a pulse generator. In this way, the input of Z = 0 (0000) to Z = 15 (1111) is set. It is to measure the time in which the output voltage Vout settles on ½ an analogue quantum . This measurement is performed for the LH and the HL transition.

HL transition:

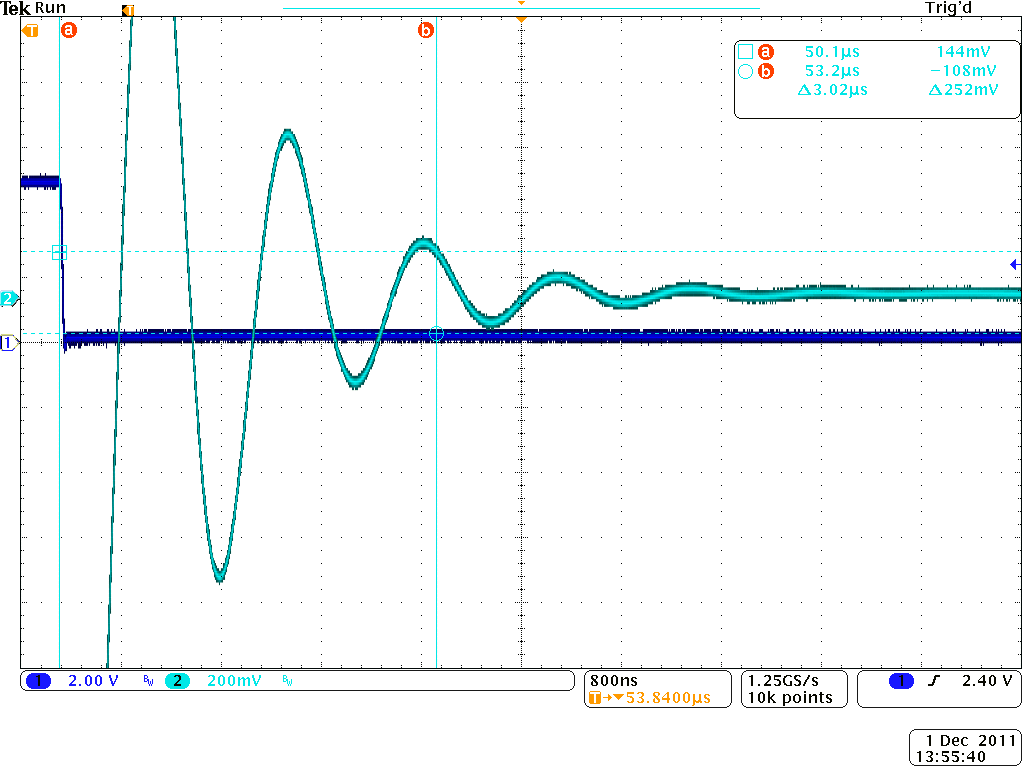


Figure 3 HL transition at the input (dark blue) and transient response of Vout (light blue)

The horizontal cursors were set at a delta of a U = 0.25V and positioned above the steady-U out. After a period of 3,02μs Vout has settled on ½ U.

LH transition:

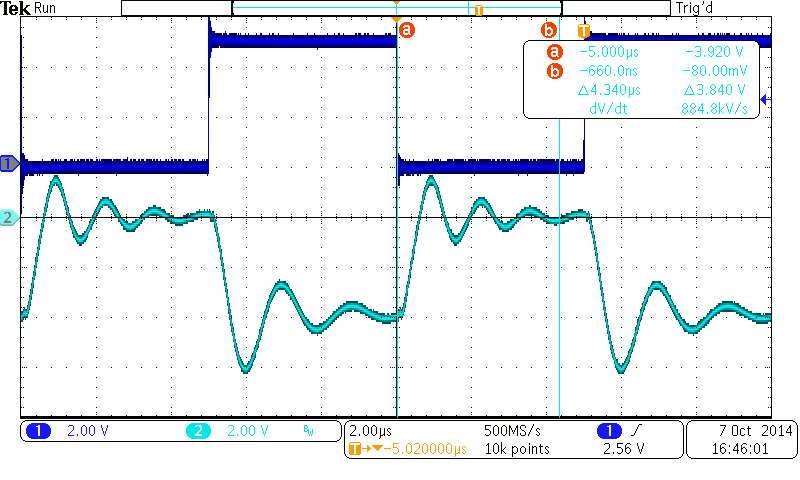


Figure 4 LH transition at the input (dark blue) and transient response of Vout (light blue)

After a period of 4,34μs Vout has settled on ½ U. This process therefore takes longer than the transient in HL transition.

## 2.2 Unipolar Binary coded 4 bit ADC­­­

We will now set up a 4-bit ADC and examines its operation. As in Experiment.



### Figure 5 Experimental setup of the 4-bit ADCs

**2.2.1 Static TransferCharacteristic**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Bit 1 | Bit 2 | Bit 3 | Bit 4 | **Uout’ [V]** |
| 0 | 0 | 0 | 0 | 0.1224 |
| 0 | 0 | 0 | 1 | 0.3672 |
| 0 | 0 | 1 | 0 | 0.6119 |
| 0 | 0 | 1 | 1 | 0.8665 |
| 0 | 1 | 0 | 0 | 1.1211 |
| 0 | 1 | 0 | 1 | 1.3659 |
| 0 | 1 | 1 | 0 | 1.6106 |
| 0 | 1 | 1 | 1 | 1.8652 |
| 1 | 0 | 0 | 0 | 2.1100 |
| 1 | 0 | 0 | 1 | 2.3743 |
| 1 | 0 | 1 | 0 | 2.6191 |
| 1 | 0 | 1 | 1 | 2.8639 |
| 1 | 1 | 0 | 0 | 3.1283 |
| 1 | 1 | 0 | 1 | 3.3828 |
| 1 | 1 | 1 | 0 | 3.6276 |
| 1 | 1 | 1 | 1 | 3.8724 |

Table 2 Measured and corrected output voltage Vout

### 2.2.2 Transient Characteristic

To the clock input CLK a pulse generator is connected, so that the 4-bit counter now counts synchronously. At varying, analog input voltage is now the voltage waveform at the non-inverting input

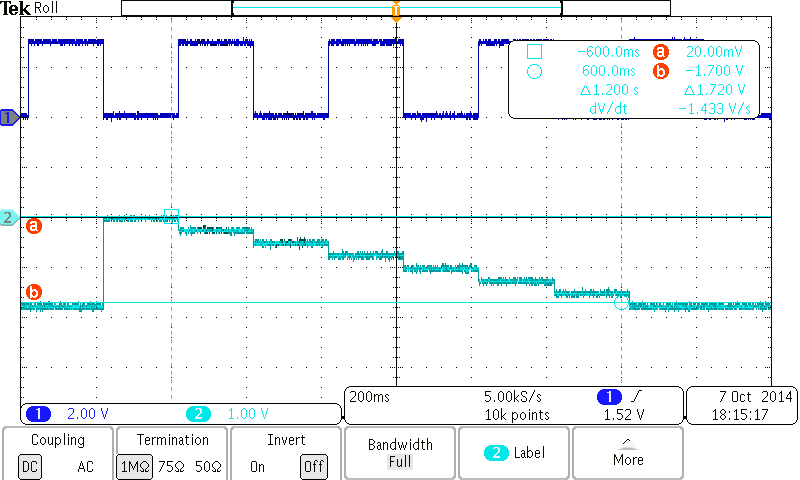


Figure 6 Stepped output voltage of the DAC

**Conclusion**

*It* occurs at this point to glitches in the stepped output voltage of the DAC, when multiple bits at the input of the DAC change state simultaneously. Is connected, for example, at the input of the DAC of "LLLL" to "HHHH", gives a very large glitch (at the beginning of the stairs). In changing the input from "HILL​​" (binary 8) to "LHHH" (binary 7) there is a visible glitch. These glitches can be attributed to the short time existing, undefined switch states that have the largest effect on the output signal when many switches are switched simultaneously.